

ASSP

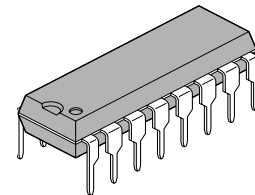
SWITCHING REGULATOR CONTROLLER

MB3769A

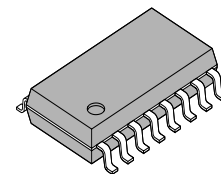
The Fujitsu MB3769A is a pulse-width-modulation controller which is applied to fixed frequency pulse modulation technique. The MB3769A contains wide band width Op-Amp and high speed comparator to construct very high speed switching regulator system up to 700 kHz. Output is suitable for power MOS FET drive owing to adoption of totem pole output.

The MB3769A provides stand-by mode at low voltage power supply when it is applied in primary control system.

- High frequency oscillator ($f = 1$ to 700 kHz)
- On-chip wide band frequency operation amplifier (BW = 8 MHz typ.)
- On-chip high speed comparator ($t_d = 120$ nsec typ.)
- Internal reference voltage generator provides a stable reference supply ($5\text{ V} \pm 2\%$)
- Low power dissipation (1.5 mA typ. at standby mode, 8 mA typ. at operating mode)
- Output current ± 100 mA (± 600 mA at peak)
- High speed switching operation ($t_r = 60$ nsec, $t_f = 30$ nsec, $C_L = 1000$ pF typ.)
- Adjustable Dead-time
- On-chip soft start and quick shut down functions
- Internal circuitry prohibits double pulse at dynamic current limit operation
- Under voltage lock out function (OFF to ON: 10 V typ. ON to OFF: 8 V typ.)
- On-chip output shut down circuit with latch function at over voltage
- On-chip Zener diode (15 V)



PLASTIC DIP 16-PIN
(DIP-16P-M04)

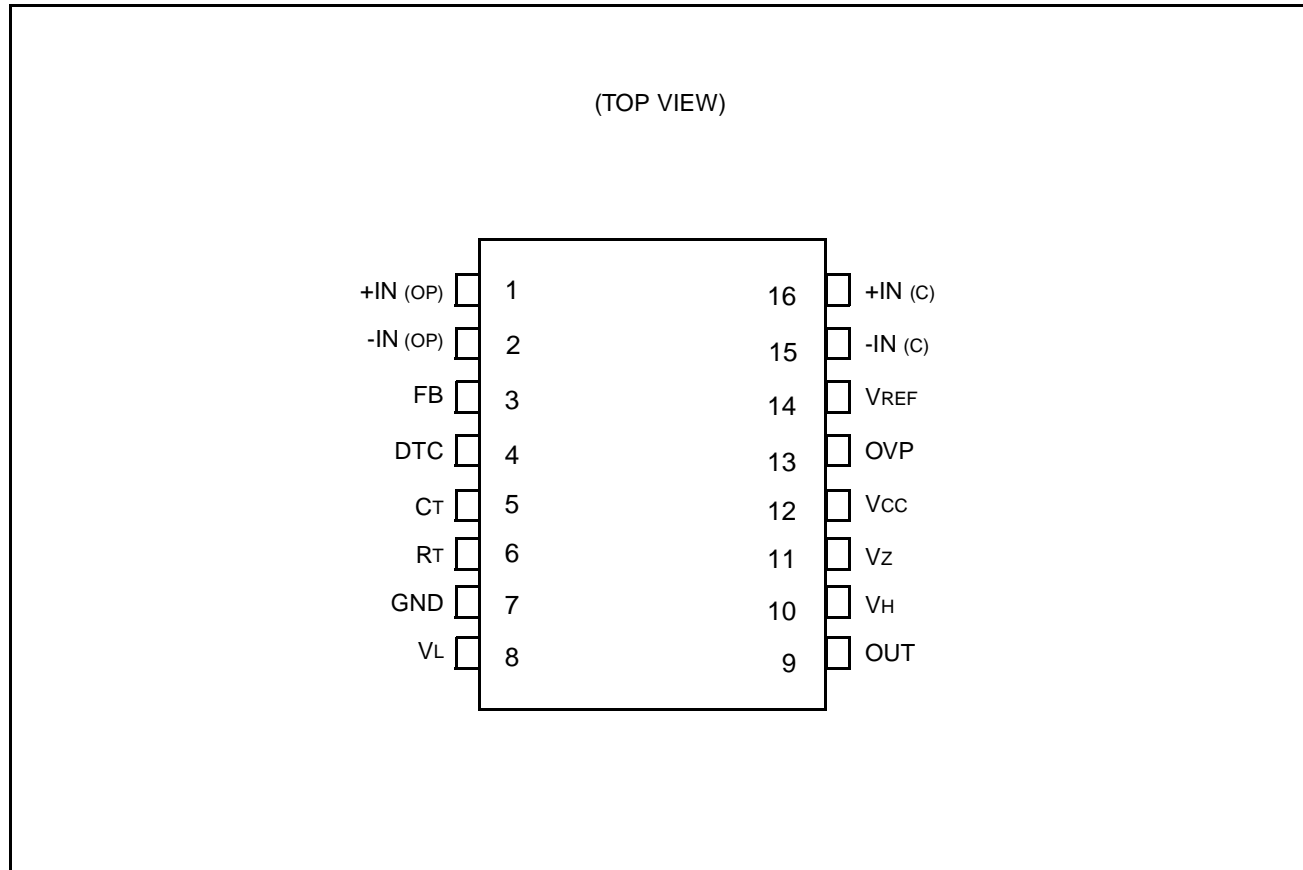


PLASTIC FPT 16-PIN
(FPT-16P-M06)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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■ PIN ASSIGNMENT



■ ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	VCC	20	V
Output Current	IOUT	120 (660*)	mA
Operation Amp. Input Voltage	Vin (OP)	VCC + 0.3 (≤ 20)	V
Power Dissipation: DIP : FPT	PD	1000**	mW
	PD	620***	mW
Operating Temp. : DIP : FPT	TOP	-30 to +85	°C
	TOP	-30 to +75	°C
Storage Temp.	TSTG	-55 to +125	°C

* : Duty $\leq 5\%$

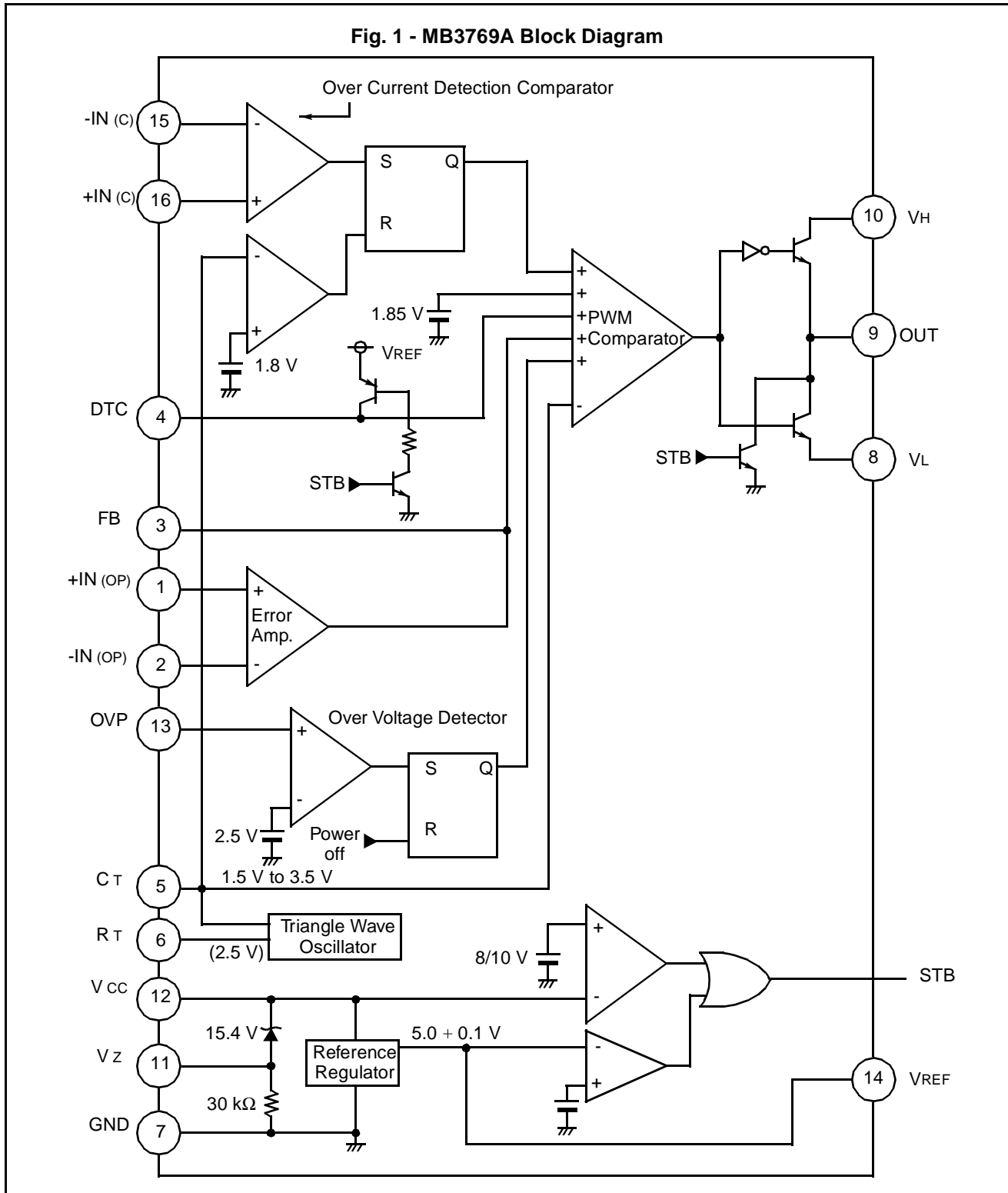
** : TA = 25 °C

*** : TA = 25 °C, FPT package is mounted on the epoxy board.
(4 cm x 4 cm x 0.15 cm)

NOTE : Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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■ BLOCK DIAGRAM



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■ RECOMMENDED OPERATING CONDITION

Parameter	Symbol	DIP package			FPT package			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage	VCC	12	15	18	12	15	18	V
Output Current (DC)	IOUT	-100	-	100	-100	-	100	mA
Output Current (Peak)	IOUT PEAK	-600	-	600	-600	-	600	mA
Operation Amp. Input voltage	VINOP	-0.2	0 to VREF	VCC -3	-0.2	0 to VREF	VCC-3	V
FB Sink Current	ISINK	-	-	0.3	-	-	0.3	mA
FB Source Current	ISOURCE	-	-	2	-	-	2	mA
Comparator Input Voltage	VINC ⁺	-0.3	0 to 3	VCC	-0.3	0 to 3	VCC	V
	VINC ⁻	-0.3	0 to 2	2.5	-0.3	0 to 2	2.5	V
Reference Section Output Current	IREF	-	5	10	-	2	10	mA
Timing Resistor	RT	9	18	50	9	18	50	kΩ
Timing Capacitor	CT	100	680	10 ⁶	100	680	10 ⁶	pF
Oscillator Frequency	fOSC	1	100	700	1	100	700	kHz
Zener Current	Iz	-	-	5	-	-	5	mA
Operating Temp.	TOP	-30	25	85	-30	25	75	°C

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=15V, T_A=25°C)

Parameter		Symbol	Condition	Value			Unit	
				Min	Typ	Max		
Reference Section	Output Voltage	V _{REF}	I _{REF} = 1 mA	4.9	5.0	5.1	V	
	Input Regulation	Δ V _{RIN}	12 V ≤ V _{CC} ≤ 18 V	-	2	15	mV	
	Load Regulation	Δ V _{RLD}	1 mA ≤ I _{REF} ≤ 10 mA	-	-1	-15	mV	
	Temp. Stability	Δ V _{RTEMP}	-30 °C ≤ T _A ≤ 85 °C	-	±200	±750	μV/ °C	
	Short Circuit Output Current	I _{SC}	V _{REF} = 0 V	15	40	-	mA	
Oscillator Section	Oscillator Frequency	f _{OSC}	R _T =18 kΩ C _T =680 pF	90	100	110	kHz	
	Voltage Stability	Δ f _{OSCIN}	12 V ≤ V _{CC} ≤ 18 V	-	±0.03	-	%	
	Temp. Stability	Δ f _{OSC} / Δ T	-30 °C ≤ T _A ≤ 85 °C	-	±2	-	%	
Dead-time Control Section	Input Bias Current	I _D		-	2	10	μA	
	Max. Duty Cycle	D _{max}	V _d = 1.5 V	75	80	85	%	
	Duty Cycle Set	D _{set}	V _d = 0.5 V _{REF}	45	50	55	%	
	Input Threshold Voltage	0% Duty Cycle	V _{DO}	-	-	3.5	3.8	V
		Max. Duty Cycle	V _{DM}	-	1.55	1.85	-	V
	Discharge Voltage	V _{DH}	V _{CC} = 7 V, I _{DTC} = -0.3 mA	4.5	-	-	V	
Error Amplifier Section	Input Offset Voltage	V _{IO (OP)}	V ₃ = 2.5 V	-	±2	±10	mV	
	Input Offset Current	I _{IO (OP)}	V ₃ = 2.5 V	-	±30	±300	nA	
	Input Bias Current	I _{IR (OP)}	V ₃ = 2.5 V	-1	-0.3	-	μA	
	Common-Mode Input Voltage	V _{CM (OP)}	12 V ≤ V _{CC} ≤ 18 V	-0.2	-	V _{CC} -3	V	
	Voltage Gain	A _{V (OP)}	0.5 V ≤ V ₃ ≤ 4 V	70	90	-	dB	
	Band Width	BW	A _v = 0dB	-	8	-	MHz	
	Slew Rate	SR	R _L = 10 kΩ, A _v = 0dB	-	6	-	V/ μsec	
	Common-Mode Rejection Rate	CMR	V _{IN} = 0 to 10 V	65	80	-	dB	
	"H" Level Output Voltage	V _{OH}	I ₃ = -2 mA	4.0	4.6	-	V	
	"L" Level Output Voltage	V _{OL}	I ₃ = 0.3 mA	-	0.1	0.5	V	

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■ ELECTRICAL CHARACTERISTICS (Continued)

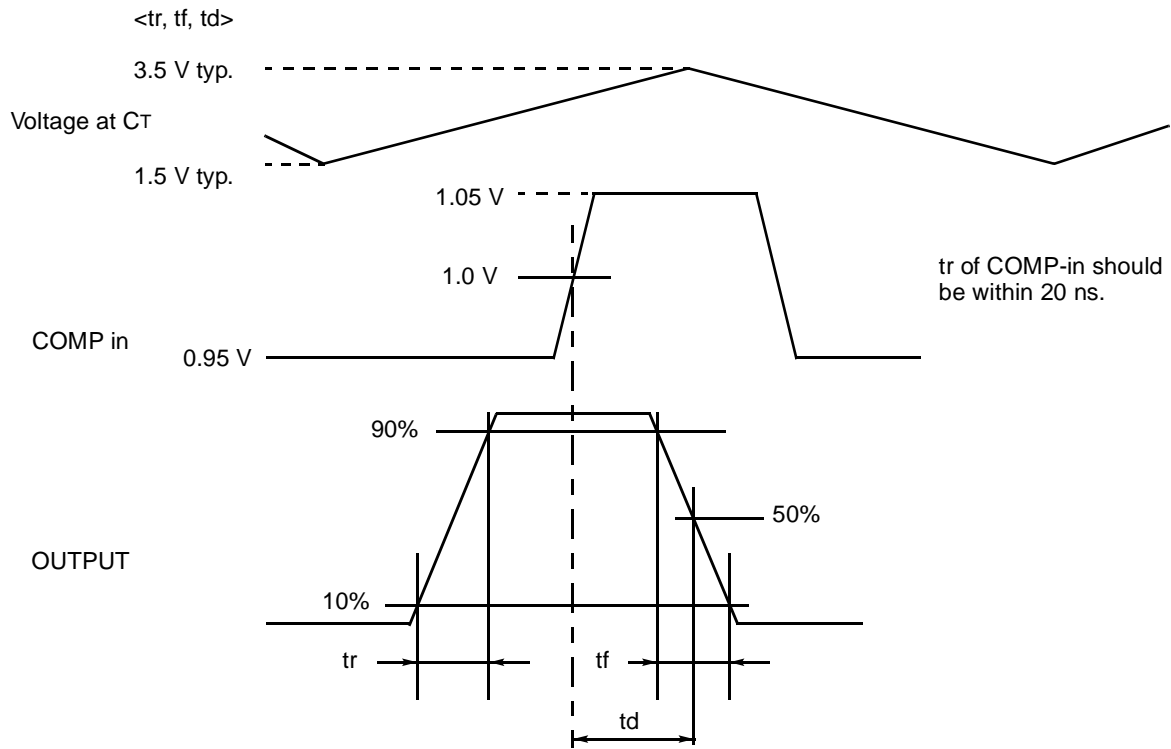
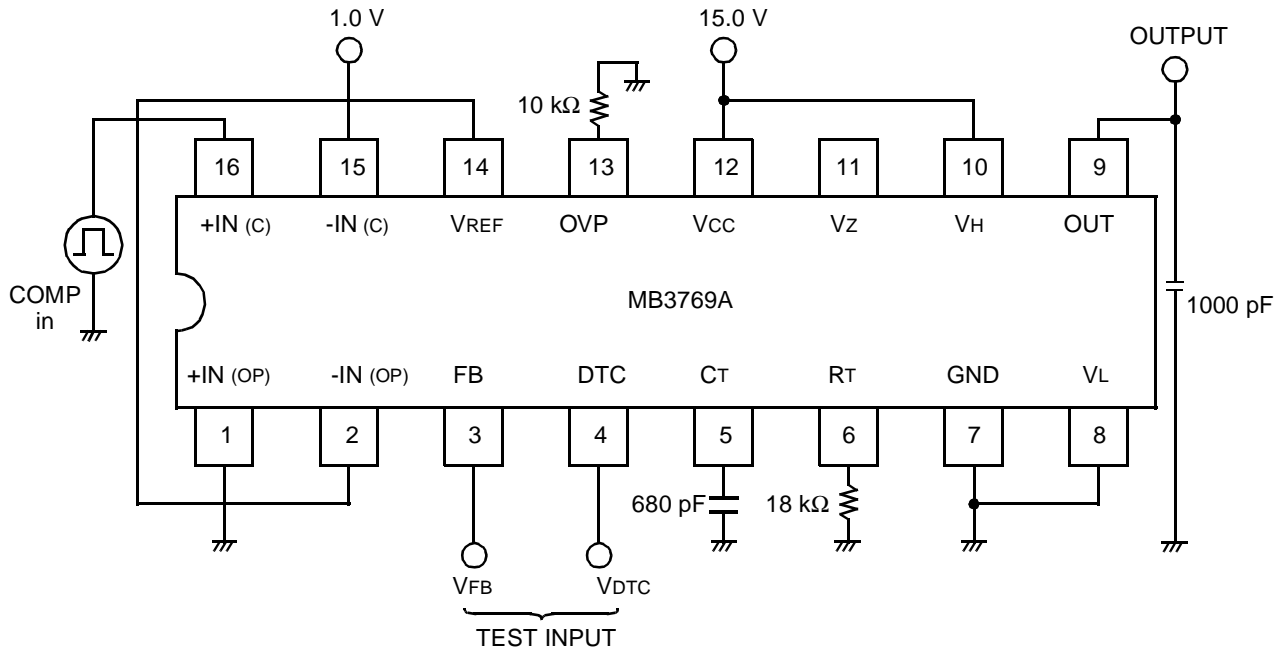
(V_{CC}=15V, T_A=25°C)

Parameter	Symbol	Condition	Value			Unit	
			Min	Typ	Max		
Current Comparator	Input Offset Voltage	V _{IO (C)}	V _{IN} = 1 V	-	±5	±15	mV
	Input Bias Current	I _{IB (C)}	V _{IN} = 1 V	-5	-1	-	μA
	Common-Mode Input Voltage	V _{CM (C)}	-	0	-	2.5	V
	Voltage Gain	A _{V (C)}	-	-	200	-	V/V
	Response Time	t _d	50 mV over drive	-	120	250	nsec
PWM Comparator Section	0% Duty Cycle	V _{OPO}	R _T = 18 kΩ C _T = 680 pF	-	3.5	3.8	V
	Max. Duty Cycle	V _{OPM}		1.55	1.85	-	V
Output Section	"H" Level Output Voltage	V _H	I _{OUT} = -100 mA	12.5	13.5	-	V
	"L" Level Output Voltage	V _L	I _{OUT} = 100 mA	-	1.1	1.3	V
	Rise Time	t _r	C _L = 1000 pF, R _L = ∞	-	60	120	nsec
	Fall Time	t _f	C _L = 1000 pF, R _L = ∞	-	30	80	nsec
Over Voltage Detector	Threshold Voltage	V _{OVP}	-	2.4	2.5	2.6	V
	Input Current	I _{OVP}	V _{IN} = 0 V	-1.0	-0.2	-	μA
	V _{CC} Reset	V _{CC RST}	-	2.0	3.0	4.5	V
Under Voltage Out Stop	Off to On	V _{THH}	-	9.2	10.0	10.8	V
	On to Off	V _{THL}	-	7.2	8.0	8.8	V
Supply Current	Standby *	I _{STB}	R _T = 18 kΩ 4 pin Open	-	1.5	2.0	mA
	Operating	I _{CC}	R _T = 18 kΩ	-	8.0	12.0	mA
	Zener Voltage	V _Z	I _Z = 1 mA	-	15.4	-	V
	Zener Current	I _Z	V ₁₁₋₇ = 1 V	-	0.03	-	mA

* : V_{CC} = 8V

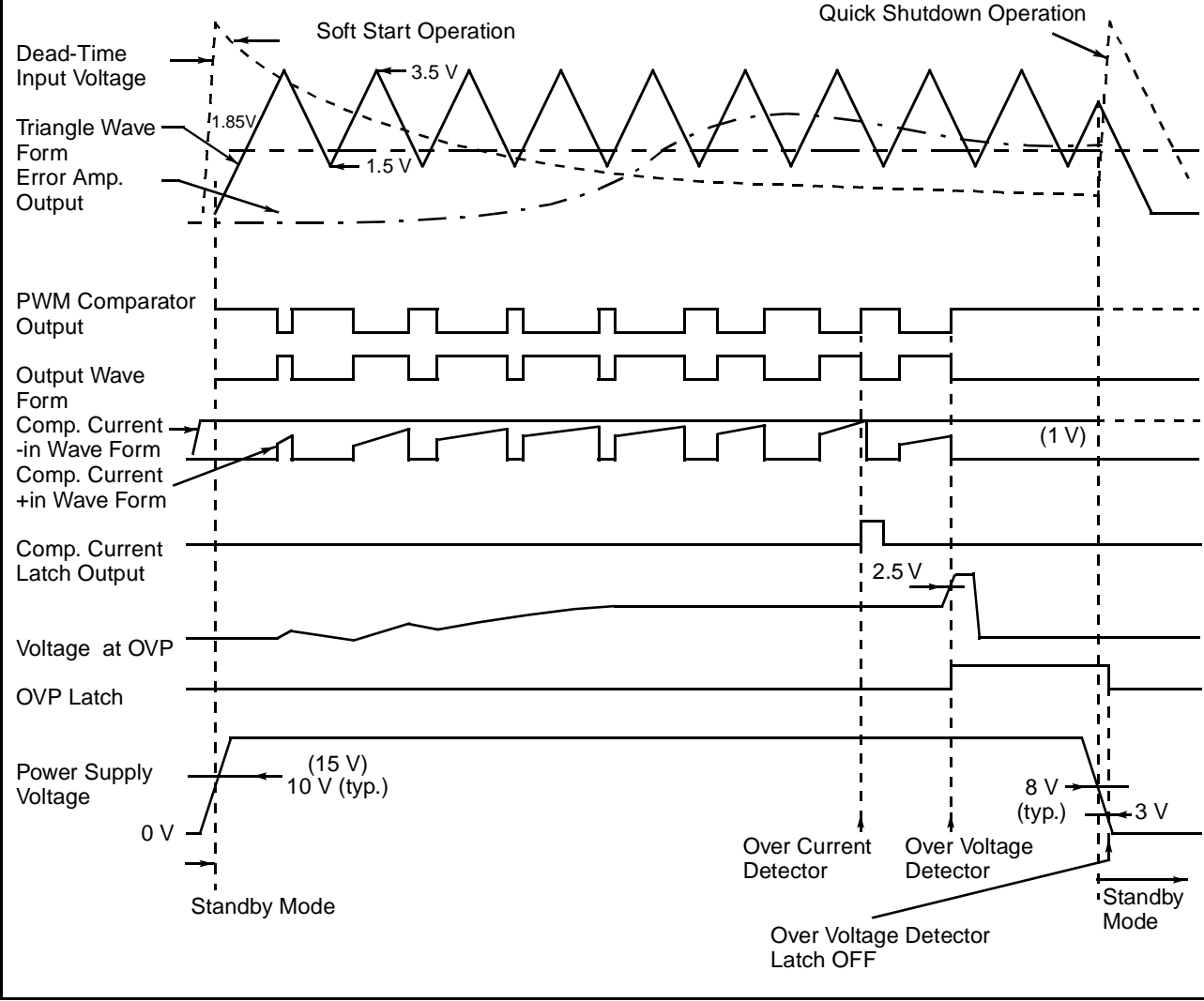
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Fig. 2 - MB3769A Test Circuit



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Fig. 3 - MB3769A Operating Timing

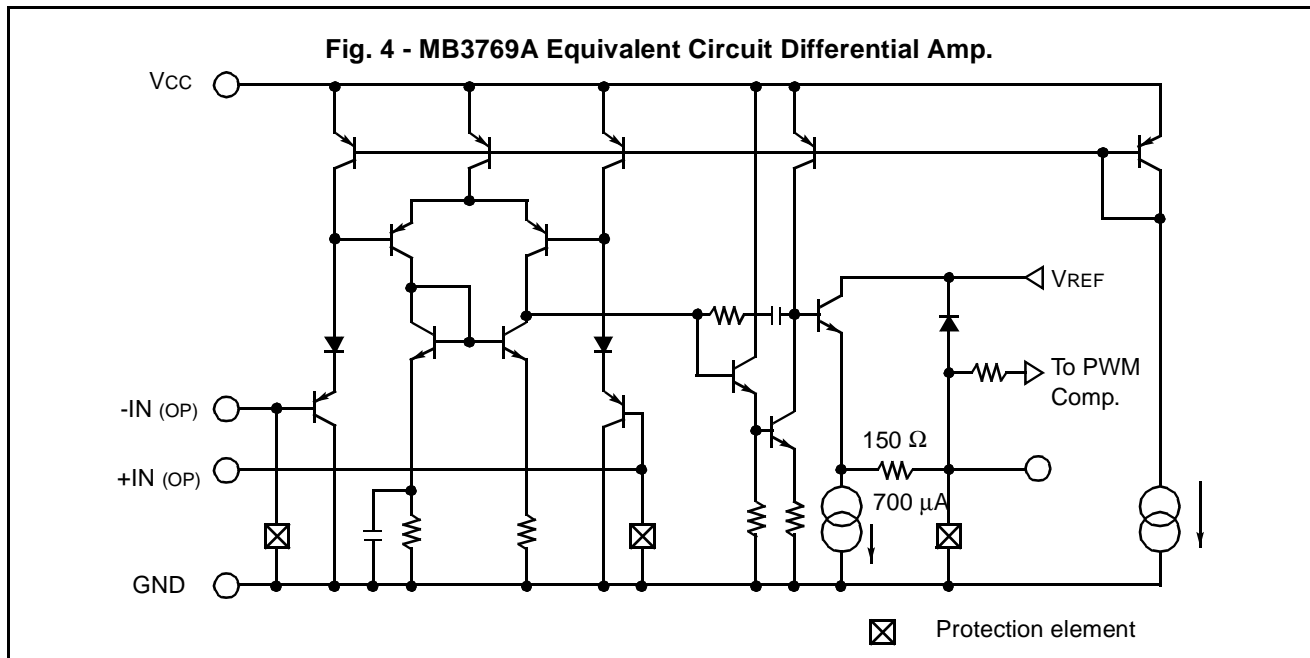


■ FUNCTIONS

1. Error Amplifier

The error amplifier detects the output voltage of the switching regulator.

The error amplifier uses a high-speed operational amplifier with an 8 MHz bandwidth (typical) and 6 V/ms slew rate (typical). For ease of use, the common mode input voltage ranges from -0.2 V to $V_{CC}-3$ V. Figure 4 shows the equivalent circuit.



2. Overcurrent Detection Comparator

There are two methods for protection of the output transistor of this device from overcurrents; one restricts the transistor's on-time if an overcurrent that flows through the output transistor is detected from an average output current, and the other detects an overcurrent in the external transistor (FET) and shuts the output down instantaneously. Using average output currents, the peak current of the external transistor (FET) cannot be detected, so an output transistor with a large safe operation area (SOA) margin is required.

For the method of detecting overcurrents in the external transistor (FET), the output transistor can be protected against a shorted filter capacitor or power-on surge current.

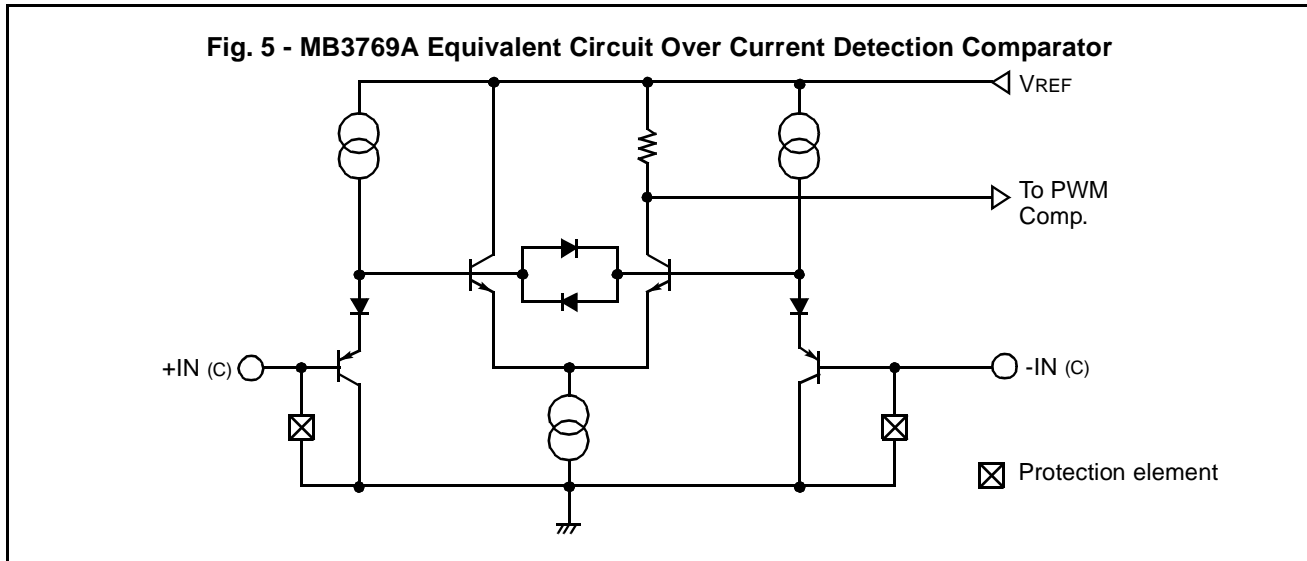
The MB3769A uses dynamic current limiting to detect overcurrents in the output transistor (FET). A high-speed comparator and flip-flop are built-in.

To detect overcurrents, compare the voltage at +IN(c) of current detection resistor connected the source of the output transistor (FET), with the reference voltage (connected to -IN(c)) using a comparator. To prevent output oscillation during overcurrent, flip-flop circuit protects against double pulses occurring within a cycle.

The output of overcurrent detector is ORed with other signals at the PWM comparator. See the example Application Example for details on use.

Figure 5 shows the equivalent circuit of the over-current detection comparator.

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3. DTC: Dead Time Control (Soft-Start and Quick Shutdown)

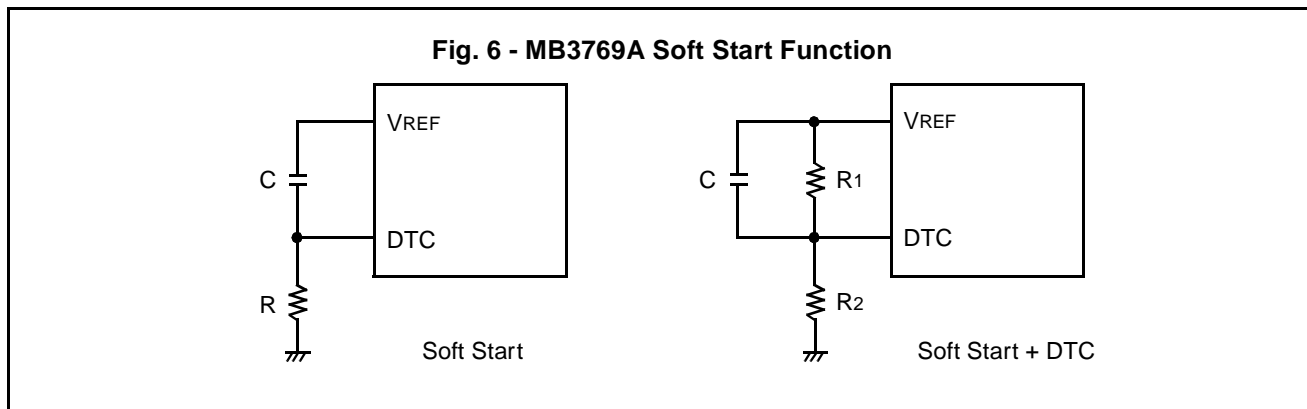
The dead time control terminal and the error amplifier output are connected to the PWM comparator.

The maximum duty cycle for VDTC (voltage applied to pin 4) is obtained from the following formula (approximate value at low frequency):

$$\text{Duty Cycle} = (3.5 - \text{VDTC}) \times 50 (\%) \quad [0\% \leq \text{duty cycle} \leq \text{D}_{\text{MAX}} (80\%)]$$

The dead time control terminal is used to provide soft start.

In Figure 6, the DTC terminal is connected to the VREF terminal through R and C. Because capacitor C does not charge instantaneously when the power is turned on, the output transistor is kept turned off. The DTC input voltage and the output pulse width increase gradually according to the RC time constant so that the control system operates safely.



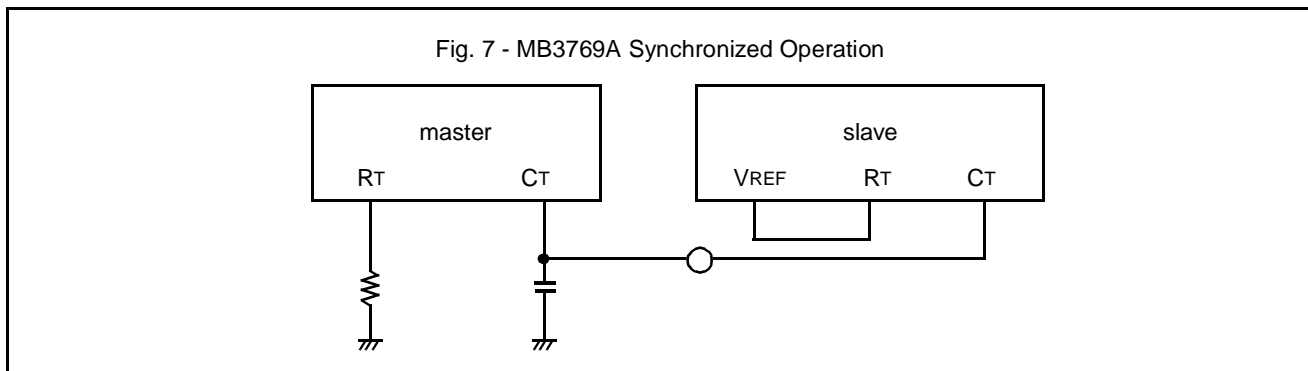
The quick shutdown function prevents soft start malfunction when the power is turned off and on quickly. After the power is shut down, soft start is disabled because the DTC terminal has low electric potential from the beginning if the power is turned on again before the capacitor is discharged. The MB3769A prevents this by turning on the discharge transistor to quickly discharge the capacitor in the stand-by mode.

4. Triangular Wave Oscillator

The oscillation frequency is expressed by the following formula:

$$f_{osc} \approx \frac{1}{0.8 \times C_T \times R_T + 0.0002 \text{ ms}} \text{ [kHz]} \quad \begin{array}{l} C_T : \mu\text{F} \\ R_T : \text{k}\Omega \end{array}$$

For master/slave synchronized operation of several MB3769As, the C_T and R_T terminals of the master MB3769A are connected in the usual way and the C_T terminals of the master and slave device (s) are connected together. The slave MB3769A's R_T terminal is connected to its V_{REF} terminal to disable the slave's oscillator. In this case, set $50/n \text{ k}\Omega$ (n is the number of master and slave ICs) to the upper limit of R_T so that internal bias currents do not stop the master oscillation.



5. Overvoltage Detector

The overvoltage detection circuit shuts the system power down if the switching regulator's output voltage is abnormal or if abnormal voltage is appeared. The reference voltage is 2.5 V ($V_{REF} / 2$). The system power is shut down if the voltage at pin 13 rises above 2.5 V . The output is kept shut down by the latching circuit until the power supply is turned off (see Figure 3).

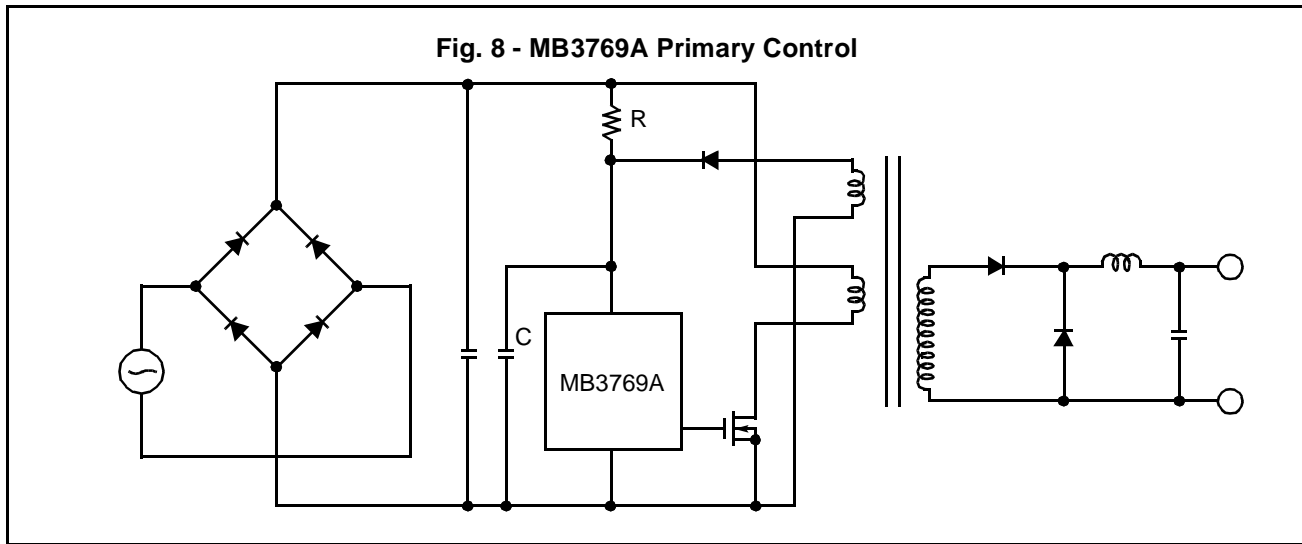
6. Stand-by Mode and Under-Voltage Lockout (UVLO)

Generally, $V_{GS} > 6$ to 8 V is required to use power MOSFET for switching. UVLO is set so that output is on at $V_{CC} \geq 10 \text{ V}$ (standard) when the power is turned on and is off at $V_{CC} \leq 8 \text{ V}$ (standard) when the power is turned off.

In the stand-by mode, the power supply current is limited to 2 mA or less when the output is inhibited by the UVLO circuit. When the MB3769A is operated from the 100 VAC line, the power supply current is supplied through resistor R (Figure 8). That is, the IC power supply current is supplied by the AC line through resistor R until operation starts. Current is then supplied from the transformer tertiary winding, eliminating the need for a second power supply.

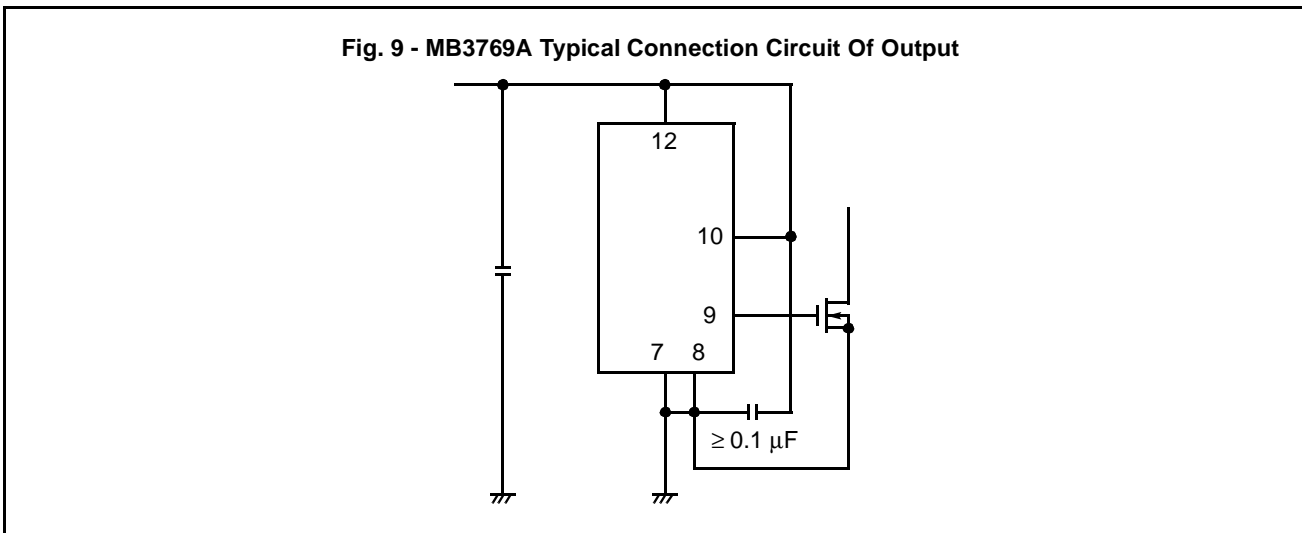
Two volts (typical) of hysteresis are provided for return from operation mode to stand-by mode not to return to stand-by mode until output power is turned on or to avoid malfunction due to noise.

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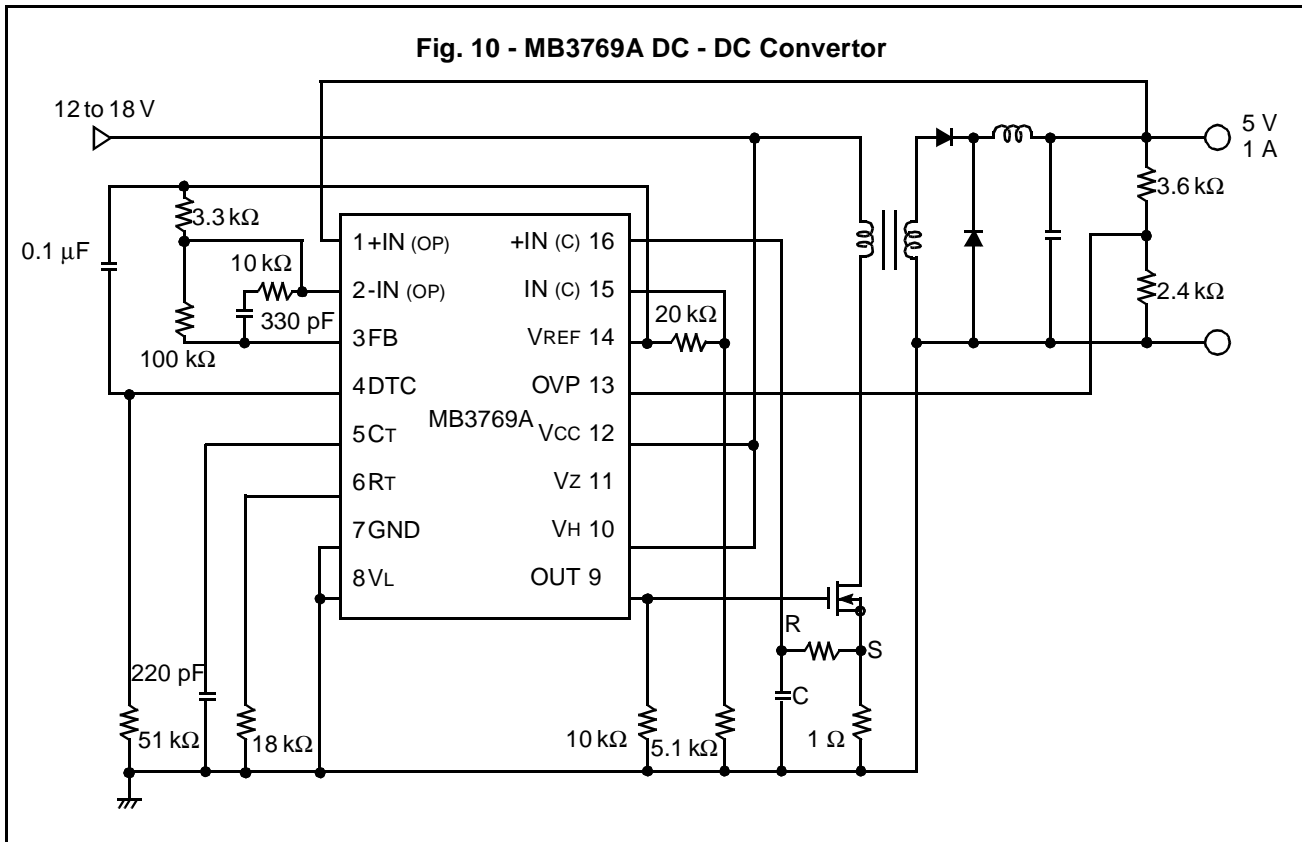
7. Output Section

Because the output terminal (pin 9) carries a large current, the collector and emitter of the output transistor are brought out to the V_H and V_L terminals. In principle, V_H is connected to V_{CC} and V_L is connected to GND , but V_H can be supplied from another power supply (4 to 18 V). Note that V_L and GND should be connected as close to the IC package as possible. A capacitor of $0.1 \mu F$ or more is inserted between V_H and V_L (see Figure 9).

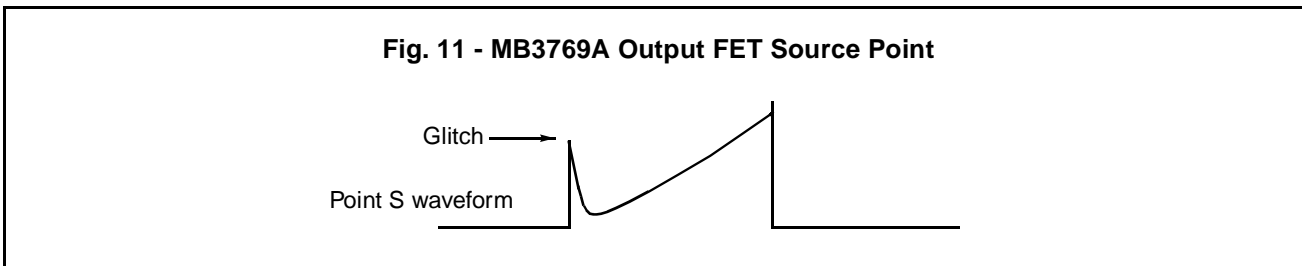


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■ APPLICATION EXAMPLE

**Overcurrent Protection Circuit**

The waveform at the output FET source terminal is shown in Figure 11. The RC time constant must be chosen so that the voltage glitch in the waveform does not cause erroneous overcurrent detection. This time constant should be from 5 to 100 ns. A detection current value depends on R or C because a waveform is weakened. To keep this glitch as small as possible, the rectifiers on the transformer secondary winding must be the fast-recovery type.



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Fig. 12 -Primary Control

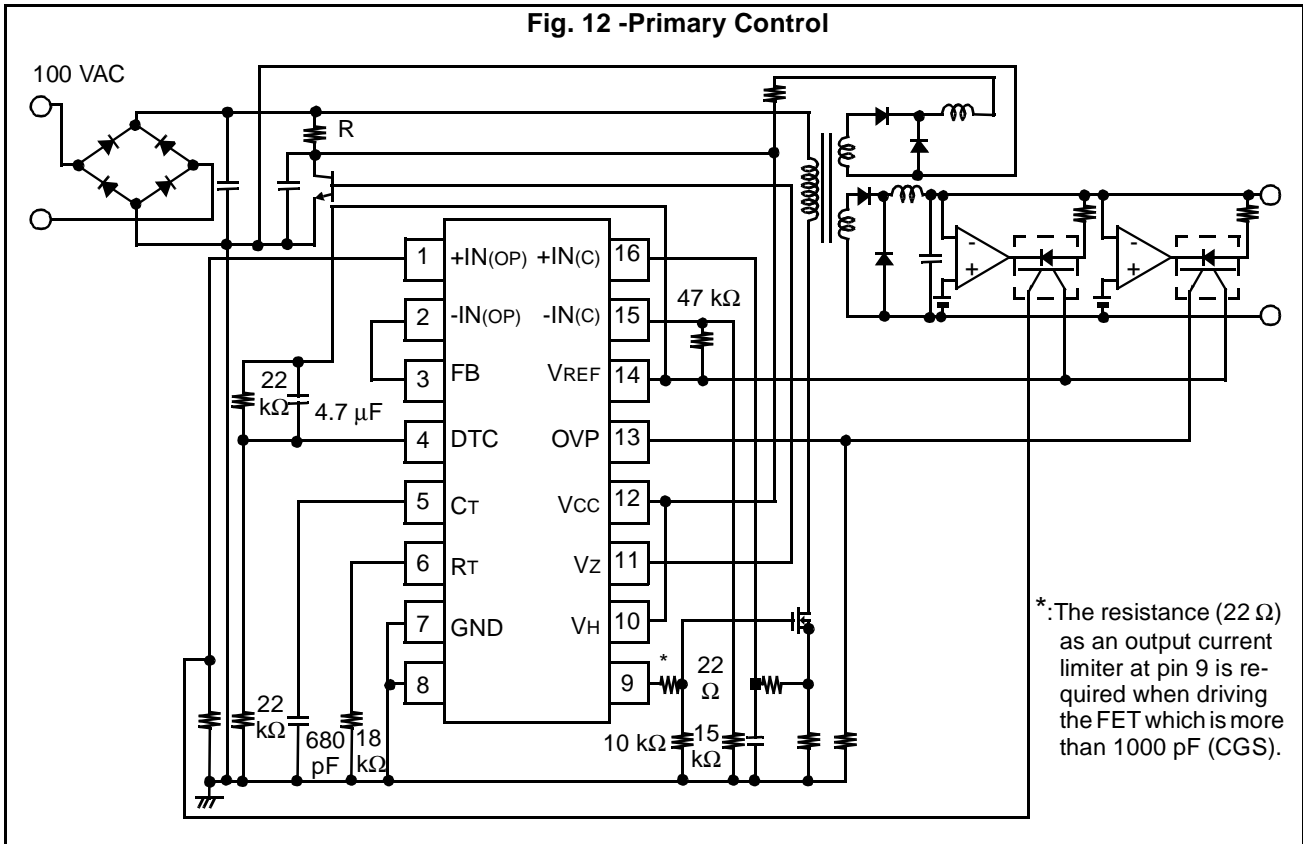
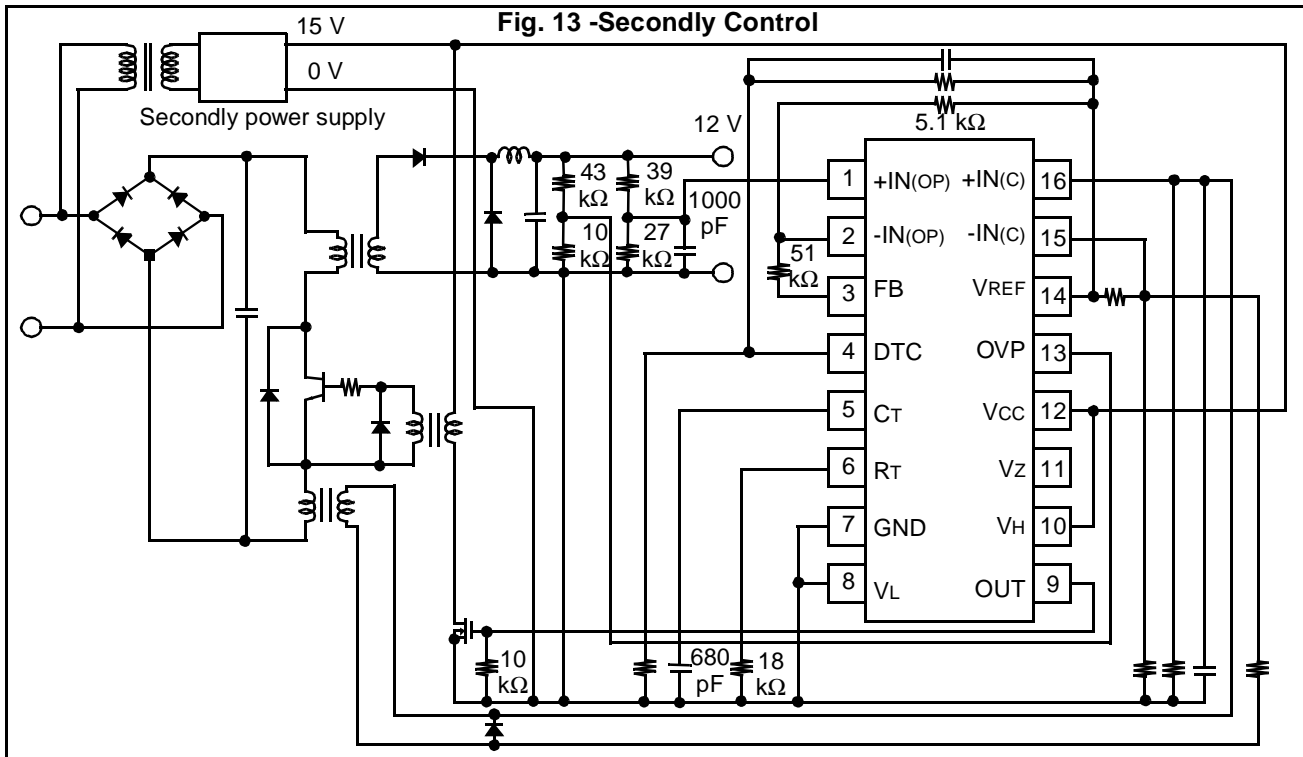
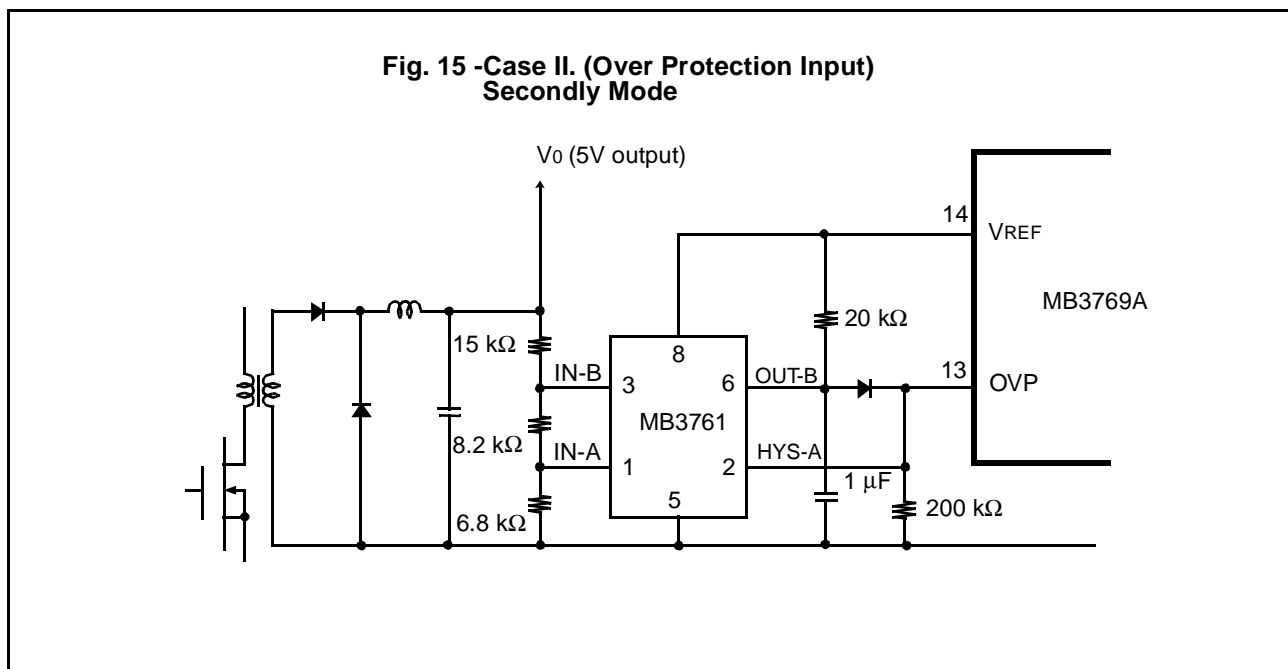
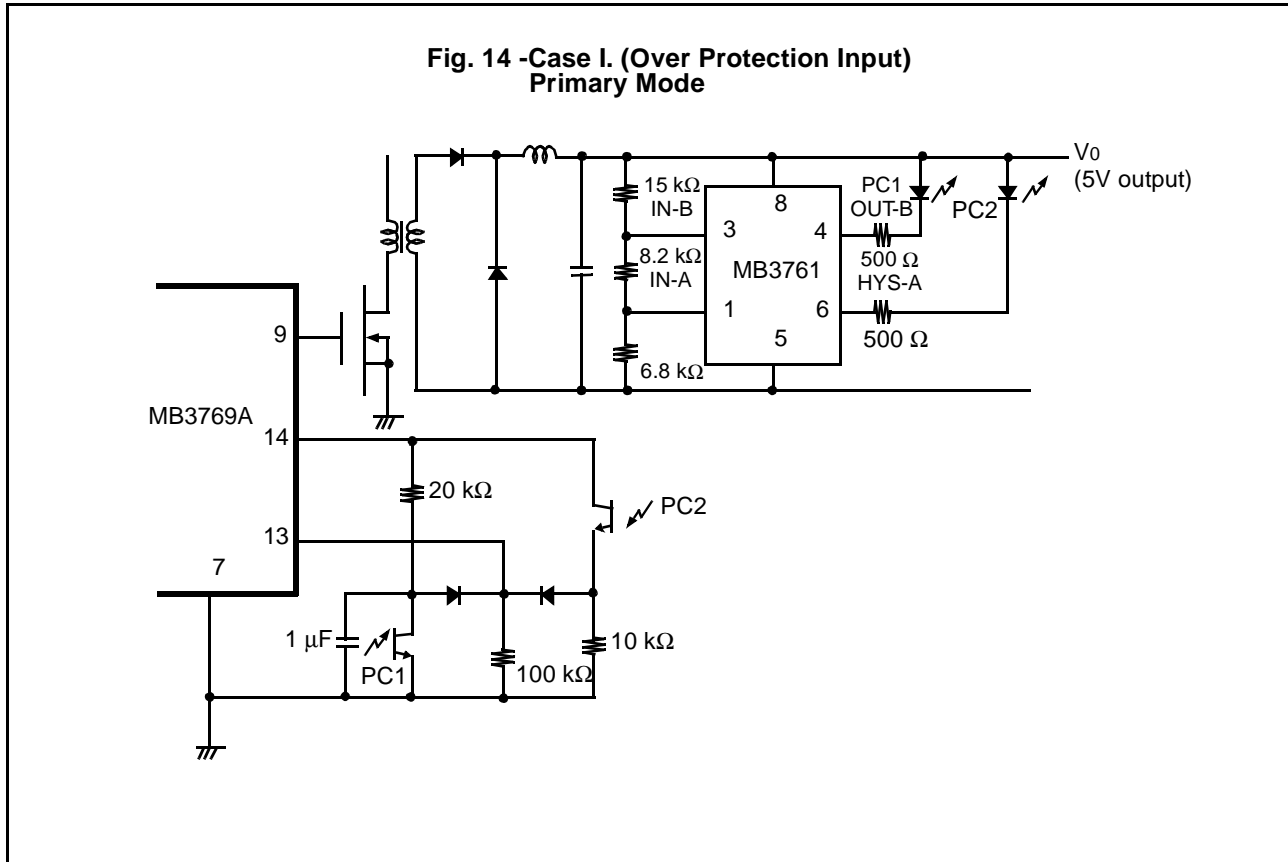


Fig. 13 -Secondly Control



■ SHORT PROTECTION CIRCUIT

The system power can be shut down to protect the output against intermittent short-circuits or continuous overloads. This protection circuit can be configured using the OVP input as shown in Figure 14.

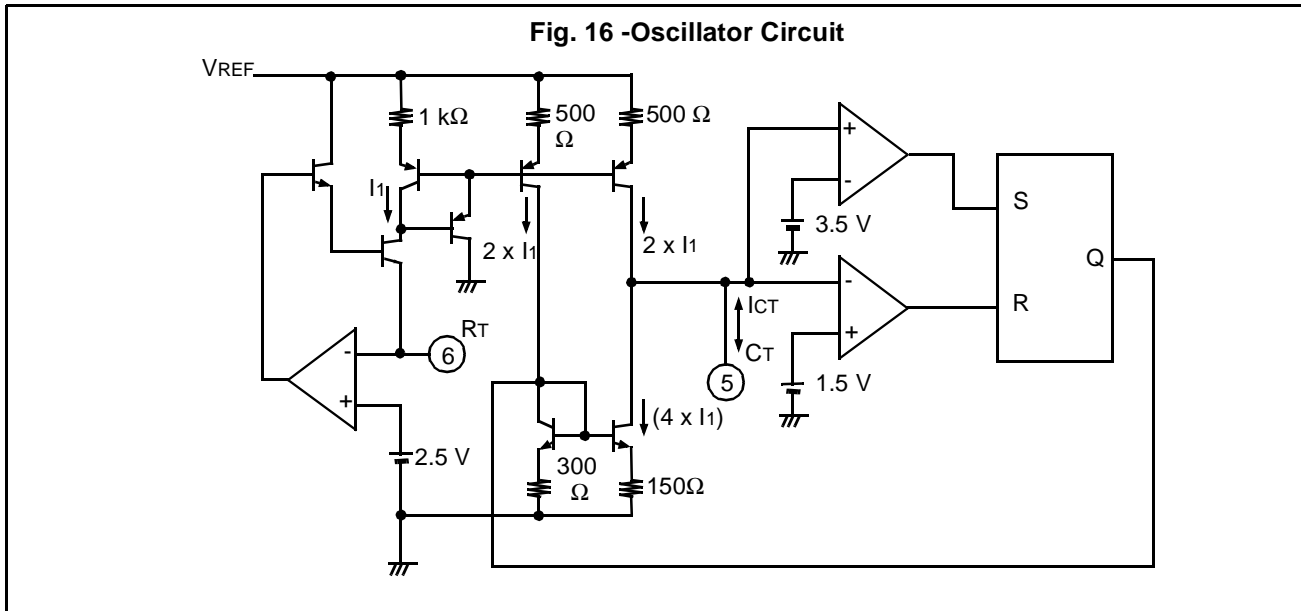


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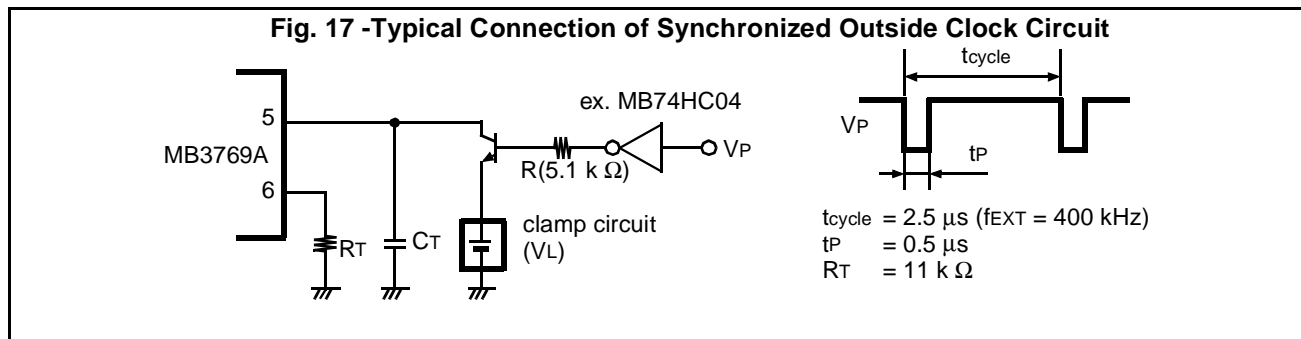
■ HOW TO SYNCHRONIZE WITH OUTSIDE CLOCK

The MB3769A oscillator circuit is shown in Figure 16. CT charge and discharge currents are expressed by the following formula:

$$I_{CT} = \pm 2 \times I_1 = \pm \frac{5V}{R_T}$$



This circuit shows that if the voltage at the CT terminal is set to 1.5 V or less, one oscillation cycle ends and the next cycle starts. An example of an external synchronous clock circuit is shown in Figure 17.



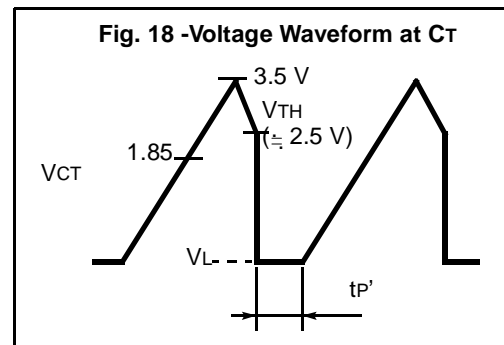
The Figure 18 shows the CT terminal waveform.

VTH may be near 2.5 V. In this case, the maximum duty cycle is restricted as shown in the formula below if tP' = 0.

$$D_{max} = \frac{(3.5 - 1.85) + (3.5 - V_{TH})}{(3.5 - V_L) + (3.5 - V_{TH})} \leq 59\% \quad (V_L = 0V: \text{ No clamp circuit})$$

When VTH = 2.5 V, CT can be provided by followings.

$$t_{cycle} - t_P = \frac{1}{f_{osc}} \times \frac{(3.5 - V_L) + (3.5 - V_{TH})}{f_{osc}(3.5 - 1.5) \times 2}$$

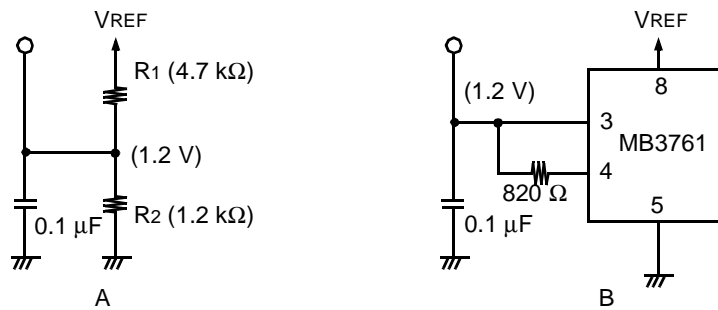


$$f_{OSC} \approx \frac{1}{0.8 \times C_T \times R_T}$$

$$C_T \approx \frac{1}{0.8 \times R_T} \times \frac{4}{4.5 - V_L} (t_{cycle} - t_P) \text{ [pF]} \quad (R_T: \text{k}\Omega, t_{cycle}, t_P: \text{ns})$$

Make V_L high for a large duty cycle for the clamp circuit. The circuits below can be used because the clamp voltage must be much lower than 1.5 V.

Fig. 19 -Clamp Circuit



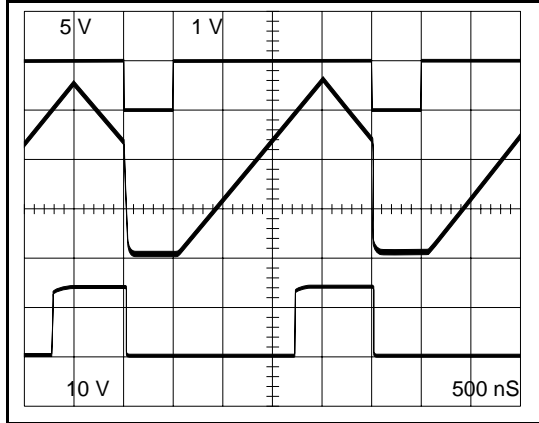
In circuit A, R_1 and R_2 must be determined considering the effects of t_P , R , or R_T .

The transistor saturation voltage must be very small (<0.15 V) for any clamp circuit, so a transistor with a very small $V_{CE(sat)}$ should be used.

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■ SYNCHRONIZED OUTSIDE CLOCK CIRCUIT

Fig. 20



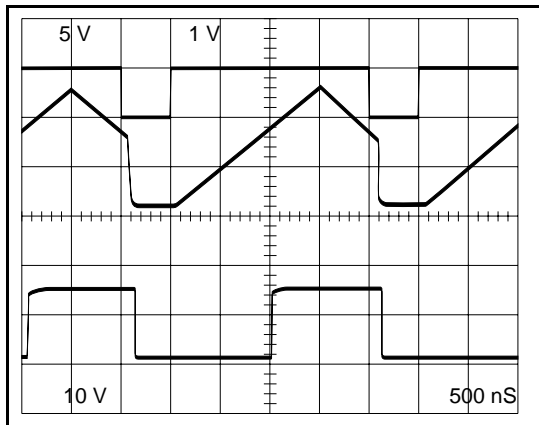
VP (5 V/div)

CT (1 V/div)

GND Level (CT)

OUT (10 V/div)

Fig. 21



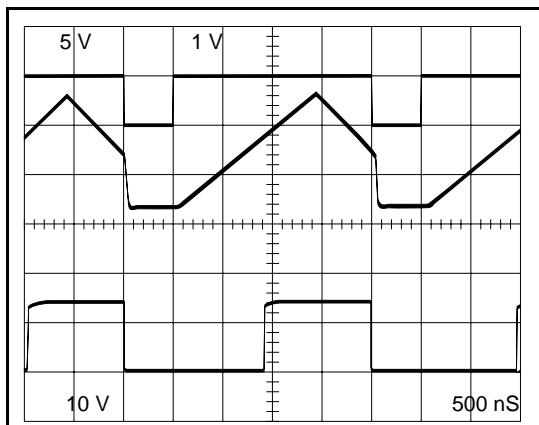
VP (5 V/div)

CT (1 V/div)

GND Level (CT)

OUT (10 V/div)

Fig. 22



VP (5 V/div)

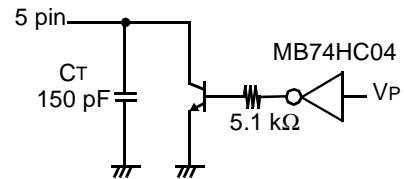
CT (1 V/div)

GND Level (CT)

OUT (10 V/div)

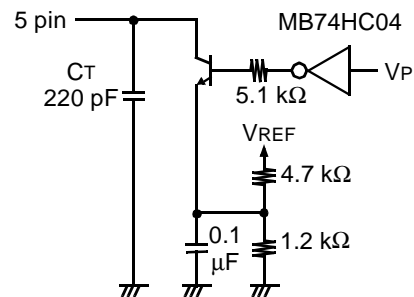
1.No Clamp Circuit (Connect with GND)

$C_T = 150 \text{ pF} + \text{Probe Capacitor } (\approx 15 \text{ pF})$
 $R_T = 11 \text{ k}\Omega$



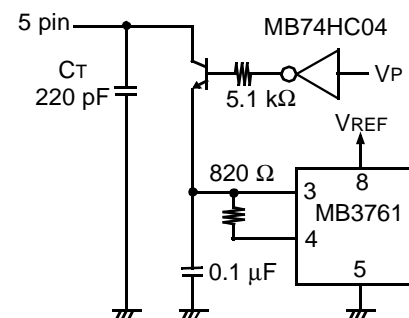
2.Clamp Circuit A (Dividing Resistor)

$C_T = 220 \text{ pF} + \text{Probe capacitor } (\approx 15 \text{ pF})$
 $R_T = 11 \text{ k}\Omega$



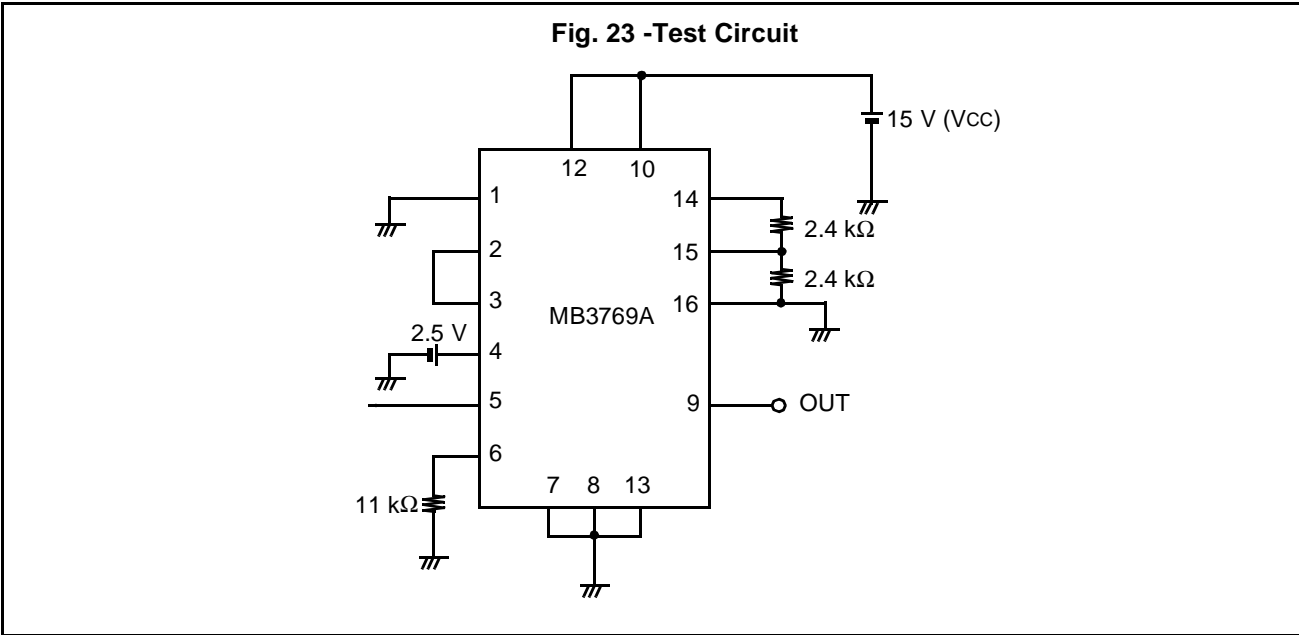
3.Clamp Circuit B (Apply MB3761)

$C_T = 220 \text{ pF} + \text{Probe capacitor } (\approx 15 \text{ pF})$
 $R_T = 11 \text{ k}\Omega$



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Fig. 23 -Test Circuit



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■ TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 24 -Power Supply Current vs. Power Supply Voltage (Low Voltage stop of V_{CC})

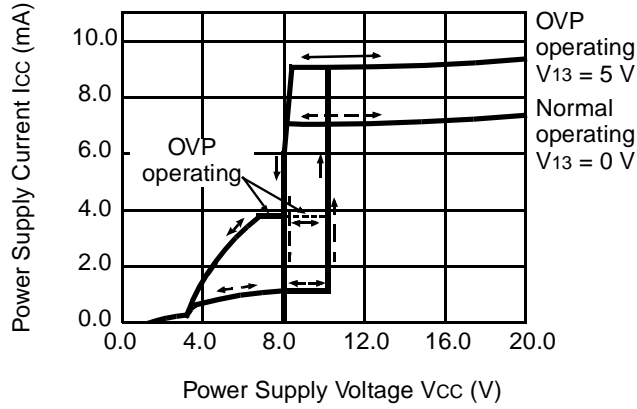


Fig. 25 -Standby Current vs.Temp.

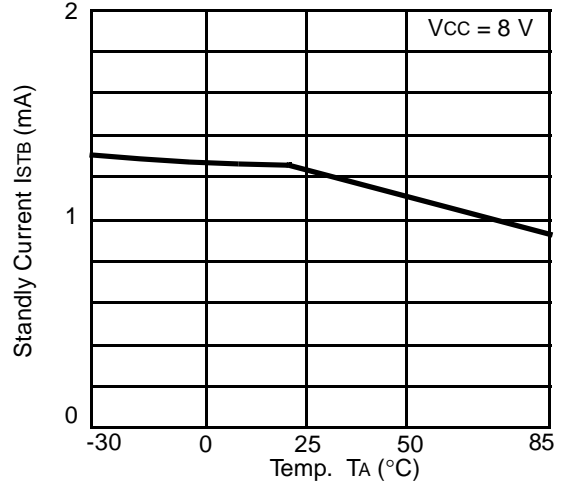


Fig. 26 -Reference Voltage vs. Temp.

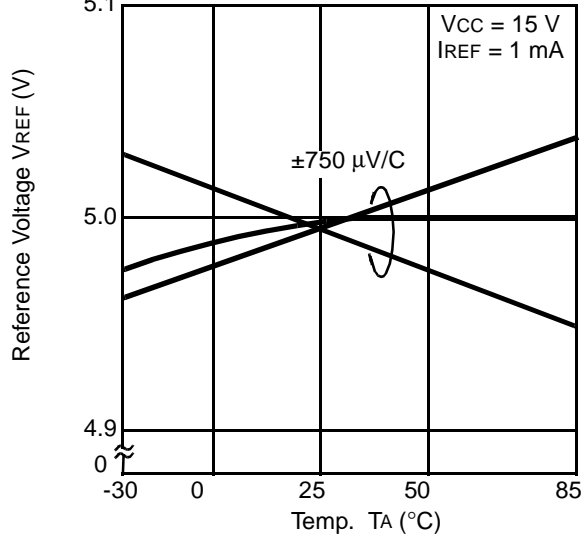


Fig. 27 -“L” level Output Voltage vs. “L” level Output Current

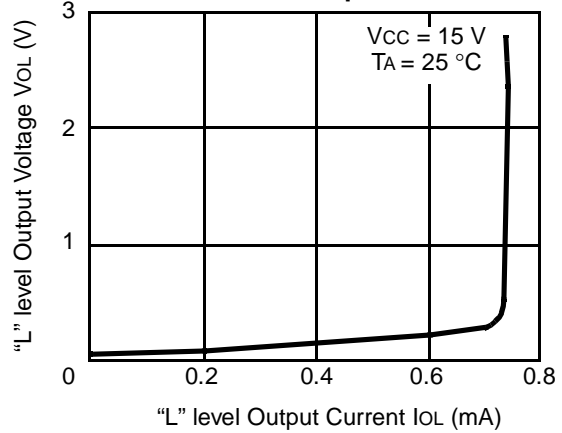
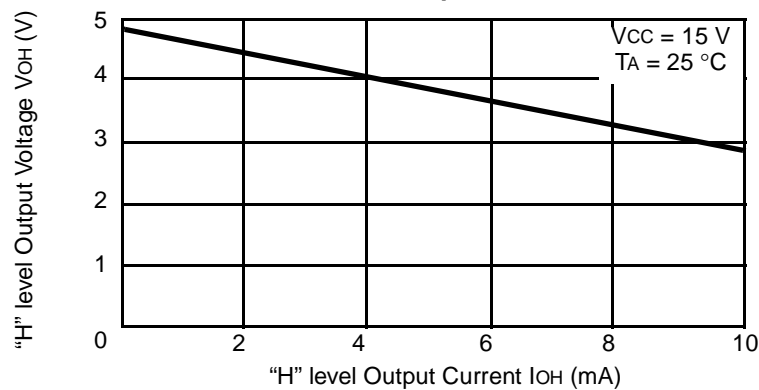
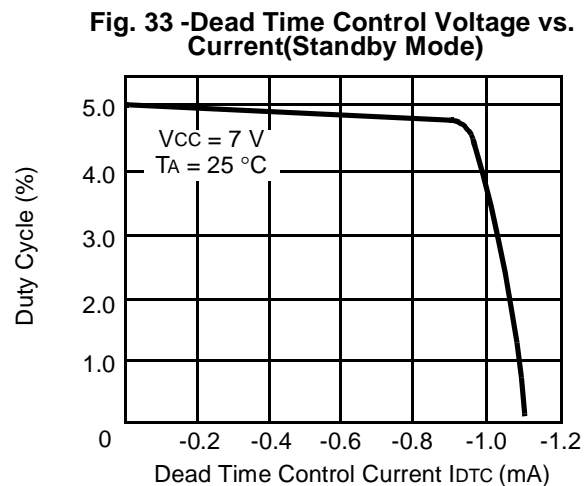
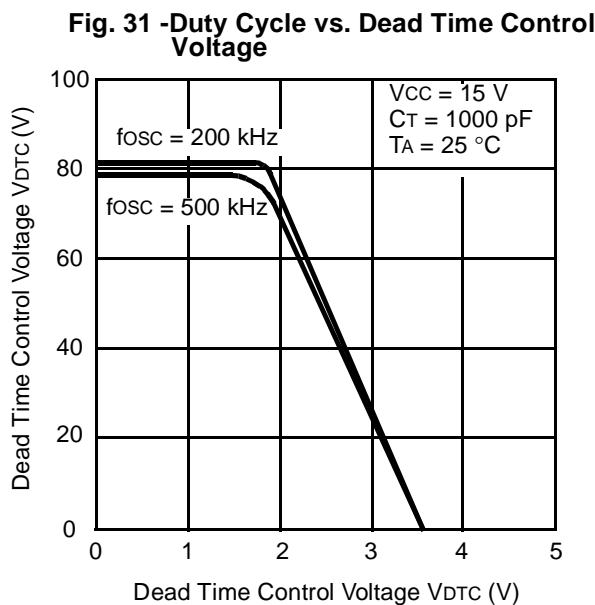
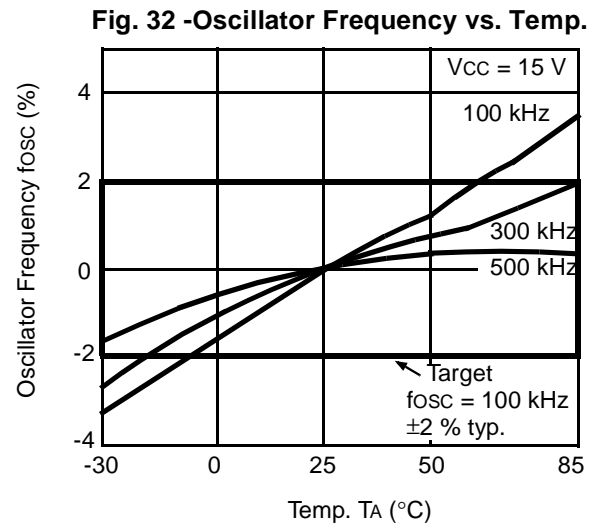
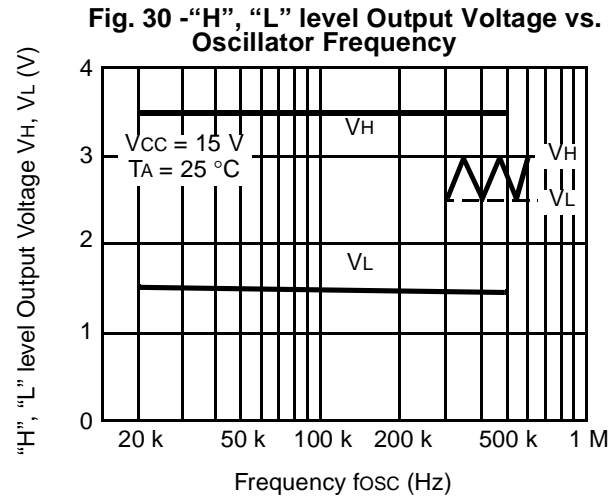
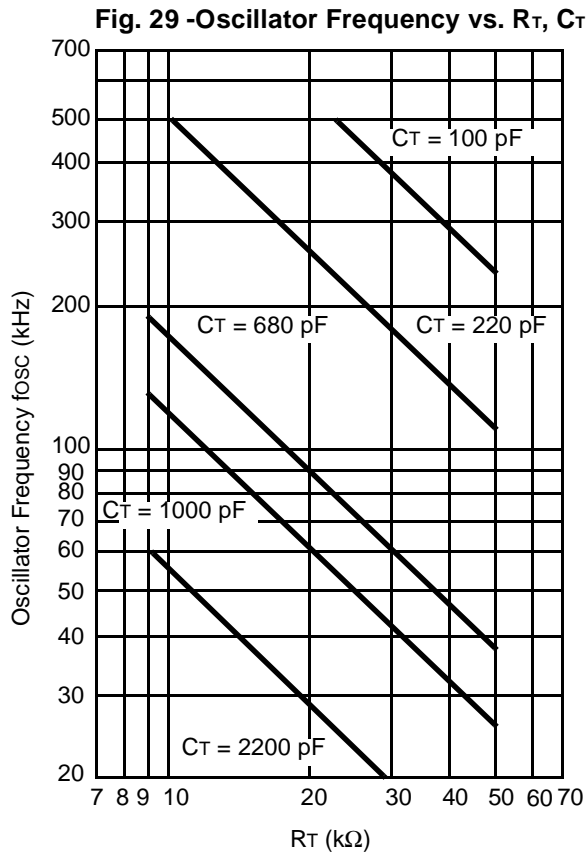


Fig. 28 -“H” level Output Voltage vs. “H” level Output Current

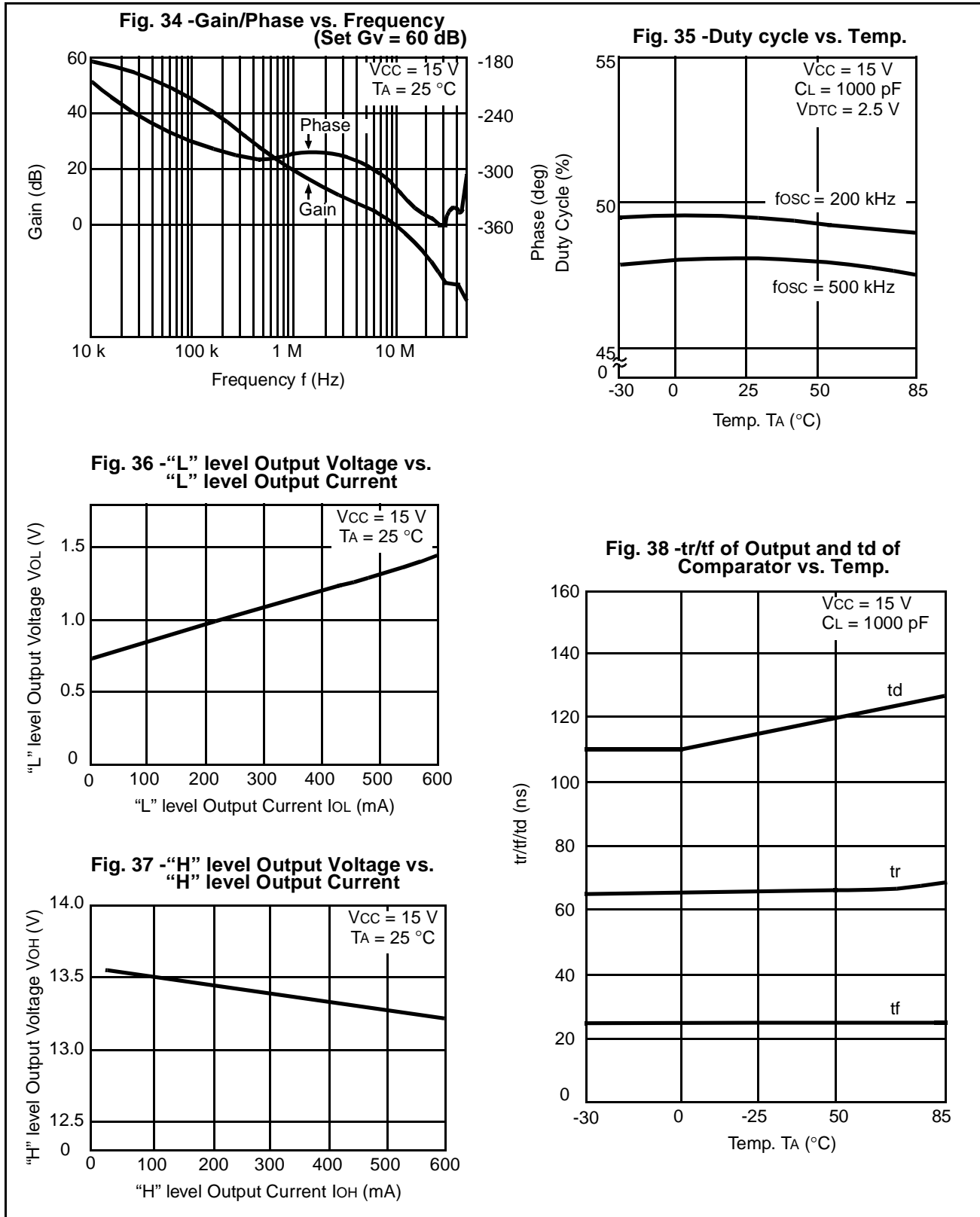


■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

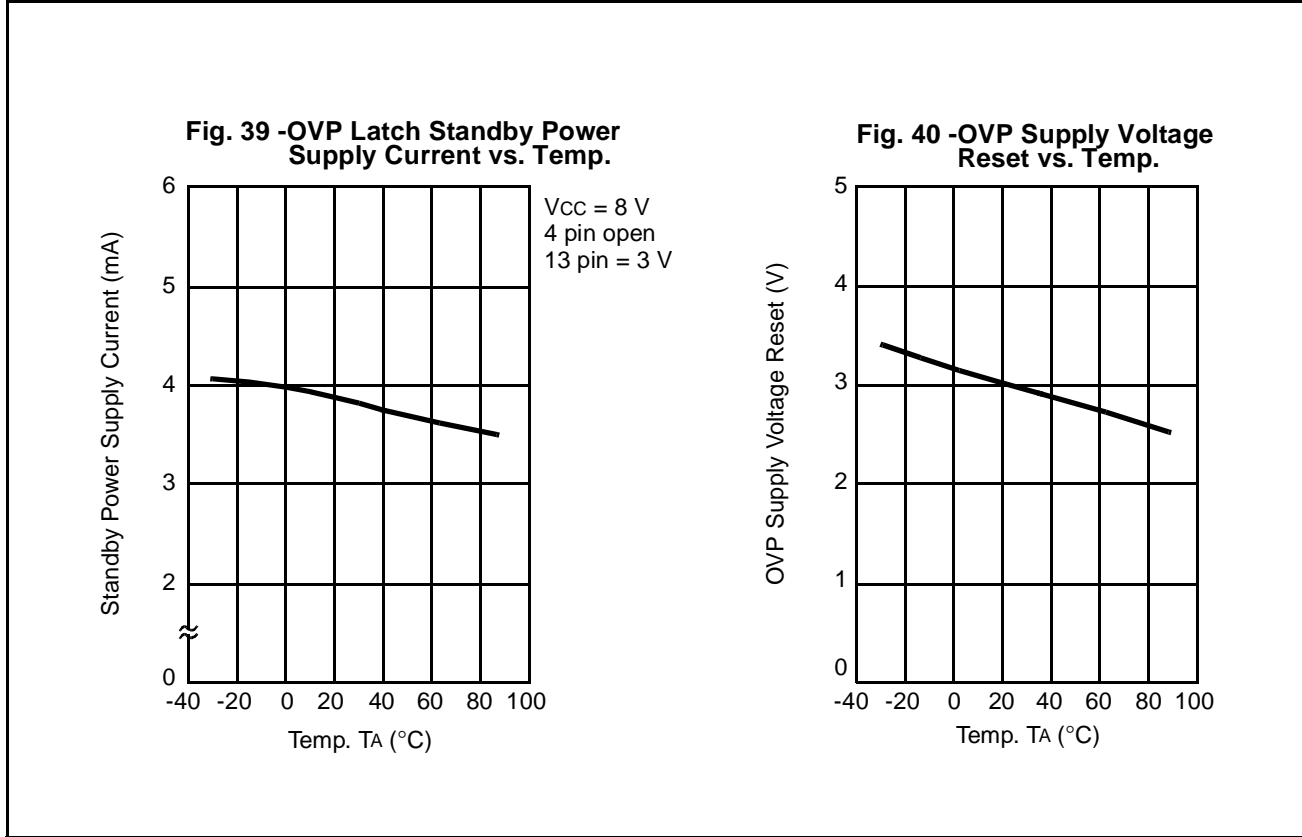


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■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



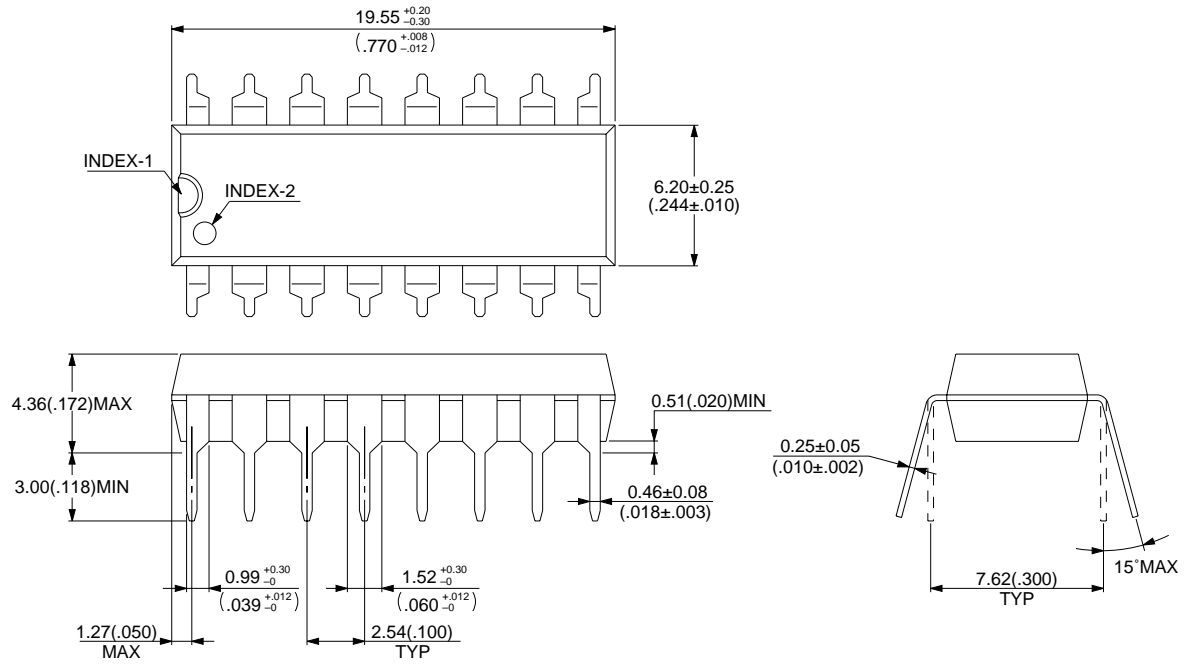
■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



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■ PACKAGE DIMENSIONS

16 pin, Plastic DIP
(DIP-16P-M04)



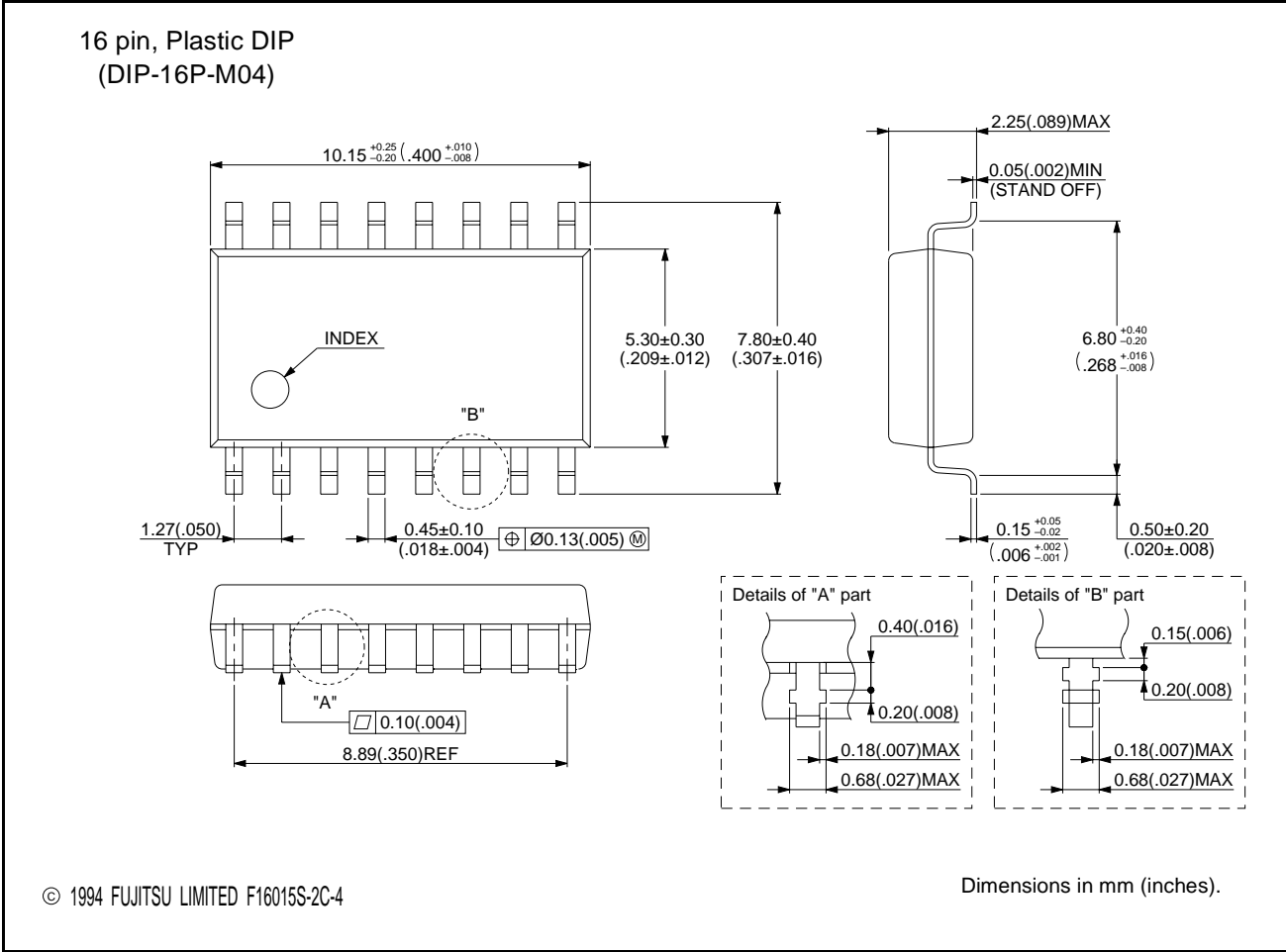
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Dimensions in mm (inches).

(Continued)

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(Continued)



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